Implementation and Algorithms for the FPD DSM Tree: Sum Version

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Description: The first two layers of DSM boards build the ADC sum for each of the 8 detector modules. All these sums are available in the third layer, which sets three thresholds on each sum. These thresholds are SIZEORDERED th0 < th1 < th2. The 4 FPD-East modules share 3 common thresholds and the 4 FPD-West modules share 3 common thresholds. For each side (East and West) and each threshold (0, 1 or 2) the 4 threshold bits are OR'ed together. All 6 bits are then sent to the last DSM. In parallel the three thresholds are coded into two bits individually for each module and these 8*2 bits are available in the scaler board. Find a drawing of the FPD-DSM tree at http://www.star.bnl.gov/STAR/html/fpdl/fy03/electronics/index.html

1. FPD-layer0, FPD-FE/W-001, 002, 003, 005, 006, 007

Input: 14x8bit ADC values from North/South Modules

Registers: None

LUT: Pedestal subtraction

Action:

1st. Clock:	Add 3*4and 1*2 PMT ADCs to intermediate ADC-Sums (adding 14 channels needs two steps)
2nd Clock:	Add intermediate sums to 12 bit ADC sum

Output (0-11) ADC sum,
(12-15) empty

2. FPD-layer0, FPD-FE/W-004

Input: 2x7 8bit ADC values; split module
North and South are swapped for East and West crate
ch0-6 East-North; West-South
ch7-13 East-South; West-North

Registers: None

LUT: Pedestal subtraction

Action:

1st. Clock:	Build intermediate ADC-Sums
2nd Clock:	Add intermediate sums to 11 bit ADC sums separately for North and South

Output (2 cables)
Lower bits East-North; West-South
(0-10) ADC sum
(11-15) empty
Upper bits East-South; West-South
(16-26) ADC sum
(27-31) empty

3. FPD-layer0, FPD-FE/W-008-010

Input: 15 8bit ADC values from Top/Bottom modules

Registers: None

LUT: Pedestal subtraction

Action:
1st. Clock: Intermediate ADC-Sums
2nd Clock: Add intermediate sums to 12 bit ADC sums

Output (0-11) ADC sum
(12-15) empty

4. FPD-layer0, FPD-FE/W-008-010

Input: 10 8bit ADC values from Top/Bottom modules

Registers: None

LUT: pedestal subtraction

Action:
1st. Clock: Intermediate ADC-Sums
2nd Clock: Add intermediate sums to 12 bit ADC sums

Output (0-11) ADC sum
(12-15) empty

5. FPD-layer1, FPD-FE/W-101, North-South modules

Both clock ticks are needed to combine 3*12 bit and 1*11bit numbers to the 14bit ADC sum of a detector module.

Input: 8xADC sums ch0-3 E-N/W-S and ch4-7 E-S/W-N

Registers: None

LUT: 1:1

Action:

1st. Clock: Intermediate ADC-Sums
2nd Clock: Add intermediate sums to 14 bit ADC sums

Output (2 cables)
Lower bits East-North; West-South
(0-13) ADC sum
(14-15) empty
Upper bits East-South; West-South
(16-29) ADC sum
(30-31) empty

6. FPD-layer1, FPD-FE/W-102, Top/Bottom

Input: 4*12bit ADC sums ch0-1 Top; ch2-3 Bottom

Registers: None

LUT: 1:1

Action:
1st. Clock: Build 13 bit ADC-Sums
2nd Clock: Delay output

Output (2 cables)
Lower bits Top
(0-12) ADC sum
(13-15) empty
Upper bits Bottom
(16-28) ADC sum
(29-31) empty

7. FPD-layer2, L1-FP201

Input: One ADC sum per detector module
ch0: East-North
ch1: East-South
ch2: East-Top
ch3: East-Bottom
ch4: West-South
ch5: West-North
ch6: West-Top
ch7: West-Bottom

Registers: **L1**: index: 11
Thresholds have to be size ordered th0 < th1 < th2!
R0: East ADC-threshold-0
R1: East ADC-threshold-1
R2: East ADC-threshold-2
R3: Logic Output Mask, 12 bits, 0-disabled, 1-enabled
Mask 11-0 is 0=output bit 0 is enabled, 1=output bit 1 is enabled, etc…

Mask 0x3f enables the “singles” (OR) outputs. 0xfc0 enables the coincidence (AND) outputs

R4: Detector Module Mask 8bits, 0-off; 1-on
Mask 7-0 is 7=BW, TW, SW, NW, BE, TE, SE, 0=NE
Mask 0x0f is east only, 0xf0 is west only
R5: West ADC-threshold-0
R6: West ADC-threshold-1
R7: West ADC-threshold-2

LUT: 1:1

Action:

1st. Clock:	Place thresholds on all input ADC sums
2nd Clock:	Code threshold comparison into scaler bits separately for all 8 modules. Two bits per module: ’00’-ADC<th0, ’01’-ADC>th0, ’10’-ADC>th1, ’11’-ADC>th2 Combine threshold comparisons for each side and each threshold and mask with bit from register 3, e.g. FPDE(0) = (NE > th0 OR SE > th0 OR TE > th0 OR BE > th0) AND R3(0)

Output (2 cables)

Lower bits to last DSM LD301
(0) Any FPD-East module > th0 AND R3(0)
(1) Any FPD-West module > th0 AND R3(1)
(2) Any FPD-East module > th1 AND R3(2)
(3) Any FPD-West module > th1 AND R3(3)
(4) Any FPD-East module > th2 AND R3(4)
(5) Any FPD-West module > th2 AND R3(5)

(6) NE > th0 AND SE > th0 AND R3(6)
(7) NW > th0 AND SW > th0 AND R3(7)

(8) NE > th2 AND NW > th2 AND R3(8)
(9) NE > th2 AND SW > th2 AND R3(9)
(10) SE > th2 AND NW > th2 AND R3(10)
(11) SE > th2 AND SW > th2 AND R3(11)
(12-15) empty

Upper bits to FPD scaler
(0-1) NE scaler bits
(2-3) SE scaler bits
(4-5) TE scaler bits
(6-7) BE scaler bits
(8-9) SW scaler bits
(10-11) NW scaler bits
(12-13) TW scaler bits
(14-15) BW scaler bits